FPGA IMPLEMENTATION OF A RECONFIGURABLE ADDRESS GENERATION UNIT FOR IMAGE PROCESSING APPLICATIONS

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Specially dedicated to my family, lecturers, fellow friends and those who have guided and inspired me throughout my journey of education

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ABSTRACT

Nowadays, the DSP algorithms are being widely used in the world of digital image processing. Example of the DSP algorithms that used in image processing is 2D correlation, 2D convolution, fast Fourier transforms, FIR filter and etc. The performance of the DSP algorithm is highly depends on its processing speed and memory bandwidth. Those algorithms require intensive data manipulation and calculation happens in parallel. The DSP algorithms also require complex address pattern calculation. The DSP processor needs to handle the data processing and also complex address calculation in the same time. The complex address pattern calculation using RISC processor is not efficient and therefore slower down the overall memory access speed. Hence, a dedicated hardware blocks to perform the address generation is essential. Such hardware known as Address Generation Unit(AGU). The prior arts of AGU have limitations as some of the AGU do not able to handle image edge condition and data reuse. Besides that, the prior art of the AGU have not been verified in the actual SOC environment. In this project, a reconfigurable AGU that targeted for 2D correlation, sum of absolute difference and Finite Impulse Response (FIR) is proposed. The proposed AGU able to take care of the image edge conditions by padding it with edge pixels. The proposed AGU also being integrated into the Altera Avalon fabric and fully verified in Altera DE2-70 FPGA. It also shows 30% to 40% improvements in the performance at certain area.

ABSTRAK

Pada masa kini, algoritma DSP digunakan secara luas dalam dunia pemprosesan imej digital. Algoritma DSP yang digunakan dalam pemprosesan imeg digital termasuk kolerasi 2D, convolution 2D, Fast Fourier Transform, penapis FIR dan lain lain. Prestasi algoritma DSP bergantung kepada kelajuan pemprosesan dan juga jalur lebar memori. Selain daripada itu, algoritma DSP juga memerlukan manipulasi data dan pengiraan alamat memori bercorak kompleks. Pemproses DSP perlu mengendalikan pemprosesan maklumat tersebut secara selari. Pemproses RISC diketahui kurang cekap dalam mengendalikan manipulasi data yang kompleks. Oleh kerana ini, blok perkakasan khusus untuk mengira alamat diperlukan. Perkakasan untuk mengira alamat dikenali sebagai Unit Generasi Alamat (AGU). Generasi AGU terlebih dahulu tidak mampu mengedalikan keadaan tepi imej dan mengguna semula data. Selain itu, generasi AGU terlebh dahulu tidak pernah disahkan dalam persekitaran SOC sebenar. Dalam projek ini, AGU yang boleh dikonfigur semula untik korelasi 2D, SAD dan penapis FIR dicadangkan. AGU tersebut berupaya mengendalikan keadaan tepi imej dan juga mengguna data semula. AGU tersebut akan dimasukkan ke dalam Altera Avalon Fabric dan dilaksanakan dalam papan Altera FPGA bermodel DE2-70. AGU yang dicadangkan juga mempunyai lebih kurang 30% ke 40% lebih laju daripada AGU terlebih dahulu dalam keadaan tertentu.